Design and Implementation of Crossbar Based Router

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Abstract – The heart of an on-chip network is the router, which undertakes crucial task of coordinating the data flow. A high speed on_chip router is designed and implemented in this paper. High speed is achieved by allowing routing function for each input port and high level of parallelism is achieved by using distributed arbiters. The designing has been done using the hardware description language VHDL in XILINX ISE tool. Its FPGA implementation is tested using Virtex-5 board.

Index Terms – SoC, IP cores.

1. INTRODUCTION

System on chips are not containing IP cores only and traditional methods for communication such as bus are not suitable solution for future System on chips. That is impossible to send signals from one end to another end within a clock cycle. Problems such as global wire delay and global synchronization will limit us. In order to overcome these problems, designer use models, techniques, and tools from network design field and apply them to System on chips design that leads to new paradigm called Network on chip. Network on chip is solution for communication architecture of future System on chips that are composed of switches and IP cores where communicate among each other through switches. Between IP cores data move in the form of packet. Network on chip is an emerging approach for the implementation of on chip communication architecture.

Fig.1 shows a basic NoC. A typical NoC consists of routers, links and network interface. Routers are used to find the destination by processing the data packets they received. It also finds the best path towards the destination. Links are wires which are used to interconnect various routers or it is used to connect router to network interface. Network interface separates the communication part from the computation part.

In this paper crossbar based router is designed and implemented**.** The main advantage of crossbar based router is its speed.

2. RELATED WORK

Network -on- Chip is an approach to interconnect various IP cores in a SoC design. In [1], W. J. Dally and B. Towles presented a general purpose on-chip inter connection network. The main advantages of on-chip interconnection network are structure, performance and modularity. NoC has an abstraction model, which is similar to the OSI model of large scale networks. In [2], L. Benini and G. De Micheli proposed a network abstraction model for NoC presented in [1]. The various layers present in the abstraction model are system layer, network interface layer, network layer and link layer. Various design constraints of NoC design are network topology, flow control and routing algorithms. In [3], T. Bjerregaard and S. Mahadevan presented all the design constraints of NoC. Store and forward, Virtual cut through and Wormhole flow control are the important flow control mechanisms for networks. In [4], Lionel M. Ni and Philip K Mckinley presented various flow control mechanisms.

3. CROSSBAR BASED ROUTER

The main parts of crossbar based router are FIFO buffer, arbiter unit, flow control unit, switch allocator unit, routing computational module and crossbar unit.

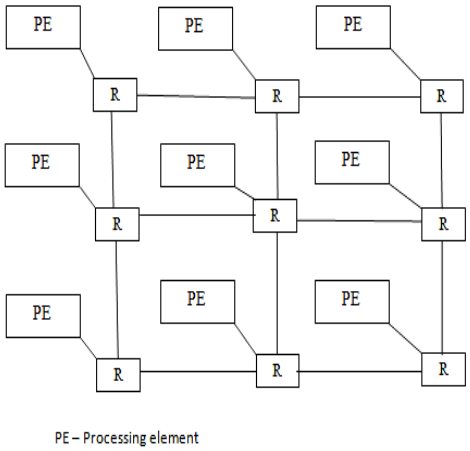

Figure 1 Basic NoC

3.1 FIFO Buffer

FIFO buffer is used to store the incoming data. Read, write, reset and clock signals are the control signals for the operation of FIFO buffer. Incoming data is the input data of the FIFO buffer. FIFO full, FIFO empty are other control signals affect the operation of FIFO buffer. We can write data to the FIFO buffer until FIFO buffer full signal goes to high. We can read data from FIFO buffer until FIFO empty signal goes to high. In

this design FIFO buffer consists of 4 rows and eight columns is used. Figure 2 shows the FIFO buffer.

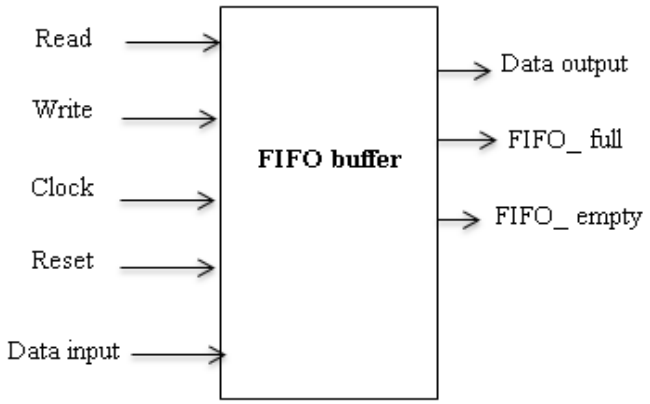

Figure 2 FIFO Buffer

3.2 Routing computational module

The routing algorithm used in this paper is XY routing. The routing algorithm determines the path between source and destination. In XY routing the source and local address is compared to find the destination. Here the address of local router is (1,1). The y co-ordinate of source is 1st compared with the y co-ordinate of local router. If the y co-ordinate is one then the x co-ordinate is compared with the x co-ordinate of local router. The XY routing algorithm is shown in table 1.

The block diagram of routing computational unit is shown in Figure 3.

3.3 Arbiter unit

In the case of router, there present multiple requests at the output port. To grant a particular request from several requests, arbiter unit is used. The arbiter unit used in this paper is round robin arbiter. This arbiter can be implemented as ring counter or FSM. In this design 5 arbiter units are present. Local arbiter, North arbiter, South arbiter, East arbiter and West arbiter. In this paper arbiter is implemented as an FSM. Figure 4 shows the block diagram of round robin arbiter.

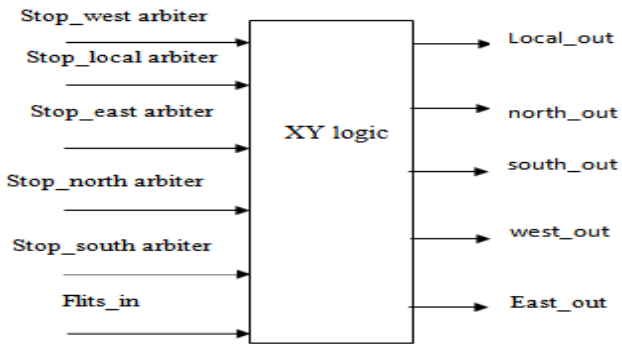

Figure 3 Routing computational module

Condition	Direction of output
Y_destination= Y_local and X_destination=X_local	Local Port
Y_destination> Y_local	East Port
Y_destination< Y_local	West Port
Y_destination= Y_local and X_destination>X_local	South Port
Y_destination= Y_local and X_destination<X_local	North Port

Table 1 XY routing algorithm

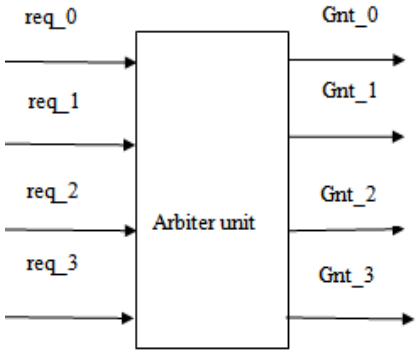

Figure 4 Arbiter unit

3.4 Switch allocator unit and crossbar switch

The switch allocator unit is used to generate the select lines for crossbar switch. The inputs for the switch allocator are grant signals from the arbiter units. The block diagram of switch allocator unit is shown in Figure 5.

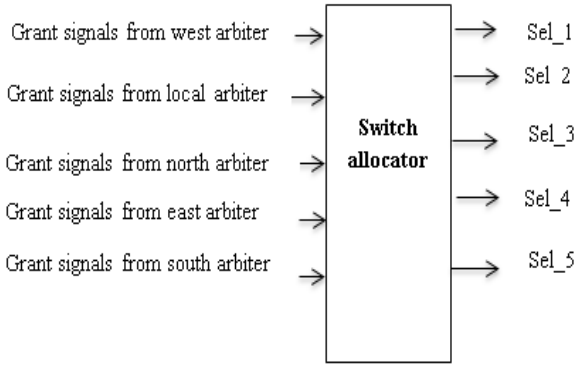

Figure 5 Switch allocator

The crossbar switch unit acts as a switch matrix to connect input port to output port. The crossbar switch consists of 5 4to1 multiplexers. The select lines for this crossbar switch are generated by the switch allocator unit. The block diagram of crossbar switch is shown in Figure 6.

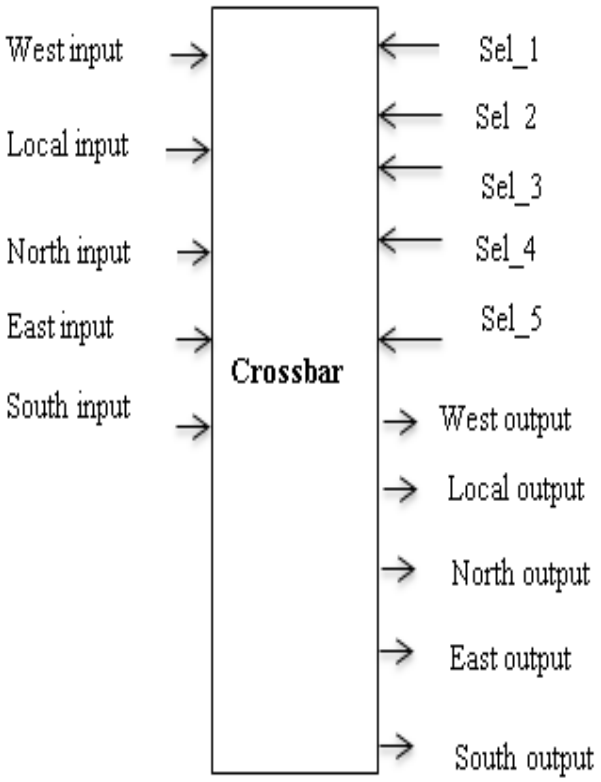

Figure 6 Crossbar Switch

3.5 Router architecture

Figure 7 shows the architecture of Crossbar based router.

4 EXPERIMENTAL RESULTS

4.1 Simulation setup

The proposed crossbar based router is designed using the hardware description language VHDL in XILINX ISE tool. In this architecture buffer size is 4. The design is simulated using Isim simulator. Simulation result of crossbar based router is shown in Figure 8.

4.2 Implementation setup

The proposed router is tested using Virtex-5 FPGA.

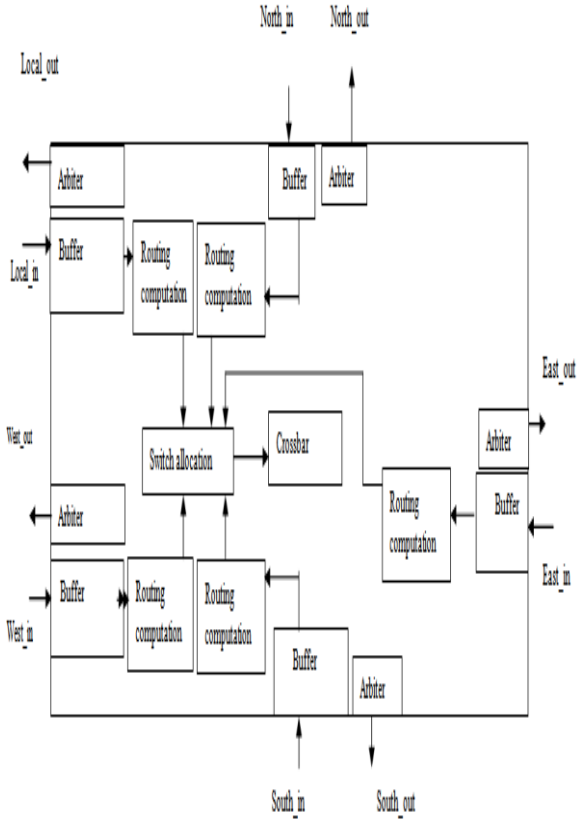

Figure 7 Crossbar based Router

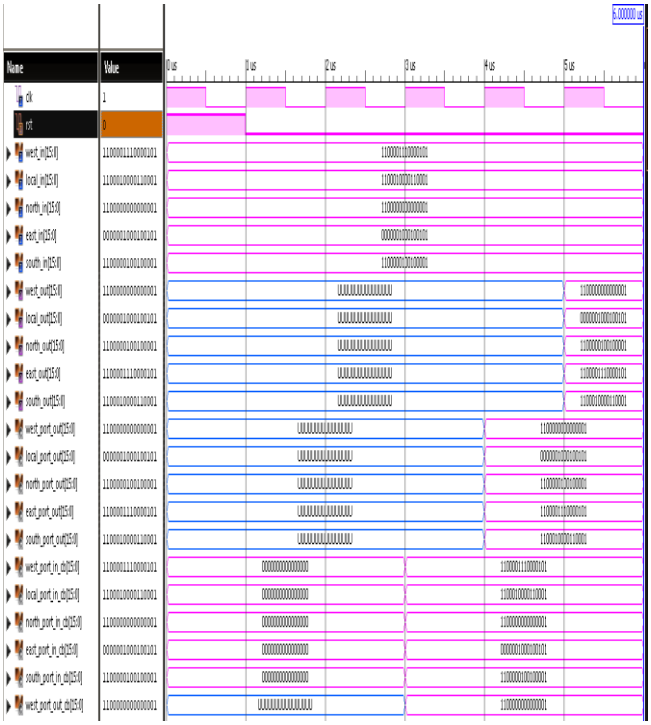

Figure 8 Simulation result of Crossbar based router

5. CONCLUSION

In this paper, I presented a Crossbar based router for network_on_Chip applications. In this paper an accurate hardware model for crossbar based router is implemented with VHDL.

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